High Electric Field Carrier Transport and Power Dissipation in Multilayer Black Phosphorus Field Effect Transistor with Dielectric Engineering

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This study addresses high electric field transport in multilayer black phosphorus (BP) field effect transistors with self-heating and thermal spreading by dielectric engineering. Interestingly, a multilayer BP device on a SiO_2 substrate exhibits a maximum current density of 3.3×10^{10} A m^{-2} at an electric field of 5.58 MV m^{-1}, several times higher than multilayer MoS_2. The breakdown thermometry analysis reveals that self-heating is impeded along the BP–dielectric interface, resulting in a thermal plateau inside the channel and eventual Joule breakdown. Using a size-dependent electro-thermal transport model, an interfacial thermal conductance of 1–10 MW m^{-2} K^{-1} is extracted for the BP–dielectric interfaces. By using hexagonal boron nitride (hBN) as a dielectric material for BP instead of thermally resistive SiO_2 ($\kappa \approx 1.4$ W m^{-1} K^{-1}), a threefold increase in breakdown power density and a relatively higher electric field endurance is obtained together with efficient and homogenous thermal spreading because hBN has superior structural and thermal compatibility with BP. The authors further confirm the results based on micro-Raman spectroscopy and atomic force microscopy, and observe that BP devices on hBN exhibit centrally localized hotspots with a breakdown temperature of 600 K, while the BP devices on SiO_2 exhibit hotspots in the vicinity of the electrode at 520 K.

1. Introduction

In pursuit of highly efficient low-power miniaturized devices, novel 2D layered materials have been explored over the last decade since conventional bulk materials have already been scaled to their geometrical dimension-performance threshold.[1,2] Interestingly, the characteristics of these layered 2D materials are dramatically different from their parent materials, especially when they are incorporated into solid state architectures. Atomically thin semiconducting 2D materials have numerous fascinating properties like mechanical flexibility, optical transparency, good electrostatic modulation, and quantum confinement.[1–3] The thicknesses of these materials are smaller than their average phonon mean free path, which is ≈50–300 nm near room temperature.[2] This has a number of effects, including: (i) the formation of abrupt junctions in their immediate environment that result in inevitable and rather frequent phonon-boundary scattering,[2,3] (ii) a significant reduction in the thermal conductivity (κ) due to a phonon confinement effect,[3] and (iii) improvements in packing density in integrated circuits and systems with increasing power dissipation density.[3,4]

Altogether, the aforementioned factors result in a substantial local temperature rise in functional devices and circuits based on 2D materials. Moreover, these devices are practically operated near current saturation conditions, i.e., under a high electric field, where charge carriers rigorously interact with each other, and also with phonons, material defects, impurities and sharp interfaces. Collectively, these scattering events further elevate the device operating temperature to a point where device breakdown occurs in a process called Joule breakdown. Heat removal is a formidable challenge that must be addressed to realize reliable operation of miniaturized devices based on novel 2D layered materials. Substantial efforts have been made under low electric field measurement conditions, but studies related to high electric fields and the corresponding power dissipation issues are rare. Therefore, we study power dissipation using high-field breakdown thermometry for field effect

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transistor (FET) architectures using 2D black phosphorus (BP) as a channel material.[5–7]

BP, a rare uni-elemental 2D material, has a sizeable, direct, and thickness-mediated optical band gap in the range of 0.3–2 eV, making it an ideal choice for numerous optoelectronic applications over a broad electromagnetic spectrum.[8] BP shows hole-dominated ambipolar behavior with a hole mobility of ≈1000 $cm^2\ V^{-1}\ s^{-1}$ and current rectification in the range of 10^2–10^5.[5–7] This addresses the shortcomings of other 2D materials like graphene and semiconducting transition metal dichalcogenides (TMDCs), which suffer from low on/off ratio and carrier mobility, respectively. Above all, BP exhibits pronounced in-plane directional anisotropy thanks to its puckered honeycomb lattice structure enabled by sp^3 hybridization between its orbitals.[6,7,9] For example, BP exhibits different in-plane κ values along its zigzag (κ_{zz} ≈ 10–20 $W\ m^{-1}\ K^{-1}$) and armchair (κ_{AC} ≈ 20–40 $W\ m^{-1}\ K^{-1}$) directions depending on flake thickness.[9] However, the average κ of BP ($\kappa_{avg} = \sqrt{\kappa_{AM} \times \kappa_{ZZ}} \approx 28.8\ W\ m^{-1} K^{-1}$) is smaller than that of graphene (>2000 $W\ m^{-1}\ K^{-1}$)[2] and MoS_2 (85 $W\ m^{-1}\ K^{-1}$)[10] due to the large disparity in its in-plane phonon modes,[9] comparatively smaller contribution of the out-of-plane acoustic modes,[11,12] and lower Debye temperature.[12] The smaller κ value of BP together with its higher electrical conductivity (σ) make it a good thermoelectric material,[13] but results in impeded heat spreading during device operation.[2–4] Therefore, it is important from a device operation and reliability perspective to have a solid understanding of high-field transport and the corresponding power dissipation issues when trying to integrate BP into energy efficient electronic structures.

Previously, Engel et al. studied the power dissipation issues in BP using micro-Raman techniques.[14] The scope of their study was limited to measure the local temperature rise during self-heating of BP flakes. In another study, the heat spreading in the BP device is reported with the heat source being optical absorption instead of Joule heating, to elucidate the thermally driven photocurrent generation.[15] In this study, we employed a simple and yet robust technique to elucidate thermal power dissipation together with efficient cooling of BP devices. We applied a high field breakdown technique to various BP FETs with different BP layer thicknesses. The applied electric field across the device was gradually increased to the point that the power deposited was large enough to cause breakdown. Our measurements showed that multilayer BP flake (11 nm) achieved a record-high current level of 603 μA ($J_{max} = 3.3 \times 10^{10}\ A\ m^{-2}$) at a maximum electric field of 5.58 $MV\ m^{-1}$. Surprisingly, the breakdown power scaled linearly with the footprint channel area ($L \times W$), which suggests that Joule heating in the channel was the likely breakdown mechanism. On the basis of this relationship, we deduced the interfacial thermal conductivity of 1–10 $MW\ m^{-2}\ K^{-1}$ between BP–dielectric interfaces.[3,16] Furthermore, our findings indicate that the poor structural and thermal properties of conventional dielectric SiO_2 limit the heat dissipation during high field transport in BP devices. Employing hexagonal boron nitride (hBN) as the dielectric material instead of SiO_2 facilitated efficient and uniform heat dissipation mainly due to its higher in-plane κ (≈360 $W\ m^{-1}\ K^{-1}$[17]) and atomically clean surface. As a result, we observed a threefold increase in breakdown power density, a relatively higher electrical field endurance, and a 13% increase in breakdown temperature for BP devices on an hBN substrate. This study provides important figures of merit and mechanisms that are crucial to improve the functionality and reliability of low power electronics, especially under harsh environments.

2. Results and Discussion

The fabricated back gate BP device, shown in the schematic diagram in **Figure 1**a and optical microscopy image in Figure 1b, was firstly characterized by applying a fixed gate bias (V_G) while sweeping the drain bias (V_D). Figure 1c shows the results obtained from a representative 11 nm-thick BP device at different gating conditions. The linearity of the plots suggests Ohmic-like contact between Cr and BP. The current level at V_G = 40 V was small, and it kept increasing as the applied V_G decreased toward −40 V. This trend confirmed p-type behavior of BP, as reported previously.[5–7] The bands tend to bend upward as V_G decreased, inducing smaller and narrower interfacial barriers for holes along the Cr–BP contacts. This resulted in an increase in current level, as indicated in the energy band diagram provided in the inset of Figure 1c. We also assembled a transfer plot of the same device, as shown in Figure 1d, which further confirms the p-type behavior with a hole current rectification ratio of ≈10^3 and hole concentration of $n_{2D} = C_{ox} \times (V_G - V_{TH}) \approx 4.4 \times 10^{12}\ cm^{-2}$ at V_G = −40 V, where C_{ox} is the capacitance per unit area to the back gate oxide ($C_{ox} = \varepsilon_0 \varepsilon_r / t_{ox} = 1.2 \times 10^{-8}\ F\ cm^{-2}$ for a 285 nm thick SiO_2) and V_{TH} (19 V) is threshold voltage of BP device. The field effect mobility was extracted from a linear fit of the data in Figure 1d using $\mu = g_m \frac{L}{W C_{ox} V_D}$. Here, g_m is the transconductance ($\partial I_D / \partial V_G$), L and W are the channel length and width, respectively. Our device had dimensions of L = 1.12 μm and W = 1.66 μm. These values resulted in a hole mobility of 267 $cm^2\ V^{-1}\ s^{-1}$ at V_D = 0.1 V under room temperature. We understand that this value can be further enhanced by optimizing flake thickness[7] and employing a high-k dielectric material.[1]

After the low-field electrical measurements, we next focused on higher electrical field (V_D/L) measurements to determine the sustainable electrical strength of BP. For these measurements, the electrical field applied to the multilayer BP device was continuously swept while gradually increasing the highest values unless electrical breakdown occurred. We observed a continual increase in current level with applied electrical field up to a certain maximum point, followed by a sudden drop in current level, as shown in **Figure 2**a. The electrical breakdown occurred soon after reaching the maximum point, so the ultimate sustainable values of current, bias, and electrical field were taken as the breakdown current (I_{BD}), breakdown voltage (V_{BD}), and breakdown field (F_{BD}), respectively. Using the 11 nm-thick BP device, we obtained an I_{BD} of 603 μA ($J_{BD} = I_{BD} / W \times t = 3.3 \times 10^{10}\ A\ m^{-2}$) at V_{BD} = 6.25 V (F_{BD} = 5.58 $MV\ m^{-1}$). Generally, an increase in current level was observed as the applied field was increased, perhaps due to the increase in drift velocity of charged carriers and their corresponding reduction of the transit time ($\text{time} = L^2 / \mu V_D$).[18] As the applied power increased, the device heated up to the extent that physical rupture, i.e., Joule breakdown, occurred.

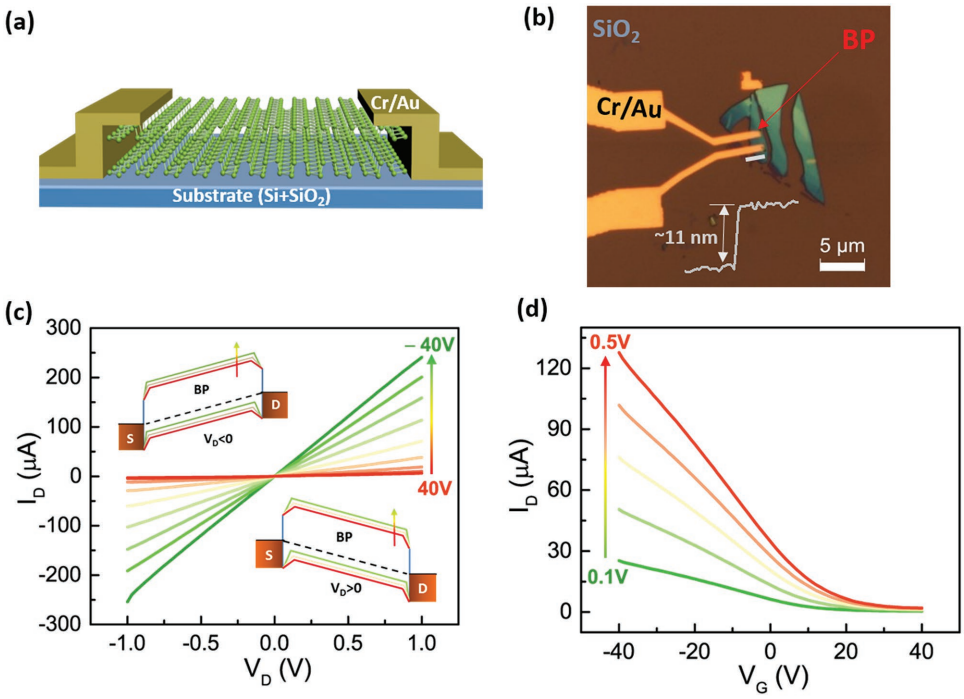

Figure 1. Low-field electrical characterization of multilayer BP device. a) Schematic of a simple two terminal back gate BP FET device. b) Optical microscope image of a representative multilayer BP device, where inset shows the AFM thickness profile along the given white line on BP flake having ≈11 nm thickness. c) Output curve of device shown in b at a different gate biases with a step of 10 V. Inset denotes the energy band diagram at different applied bias conditions. The color code indicates different gating conditions, while the upper left and lower right diagrams represent the band position at negative and positive V_D conditions, respectively. d) Transfer curve at various drain biases (0.1 V steps).

The ultimate current carrying capacity of our ≈11 nm thick BP FET, 3.3×10^{10} A m^{-2}, is around seven times higher than the maximum reported value for multilayer MoS_2 in a similar geometry,[19] and was 3.3 times higher than the basic electron-migration limits for metals.[20,21]

In addition, we studied the thickness dependence of breakdown current in multilayer BP devices. In order to accomplish this, we fabricated various two terminal BP devices with different thicknesses (all having an ≈1 μm long channel), and we measured their breakdown current (I_{BD}/W) at $V_G = 0$ as shown in Figure 2b. Interestingly, among our studied devices, the highest current level of 666 μA μm^{-1} was recorded for the 41 nm thick sample. Previous results showed that thicker BP flakes exhibited higher κ values and less surface scattering when compared to thinner flakes,[9] and this better explains the efficient thermal spreading for thicker BP samples. Therefore, an increase in ultimate current level with increasing thickness is observed. Note that I_{BD} did not scale linearly with the thickness of BP flakes since the current distribution per layer was nonuniform in the multilayer BP, mainly due to charge screening and interlayer effects as observed for MoS_2 previously.[19,22] Afterwards, we studied the effect of lateral device dimensions (L and W) on the electrical breakdown of BP. We initially fabricated devices with different L values, which were fabricated on the same BP flake, as shown in the inset of Figure 2c, and recorded their corresponding breakdown power (P_{BD}) (i.e., the product of I_{BD} and V_{BD}). Surprisingly, we found that the maximum power sustained by the BP FETs scaled linearly with L. However, a similar trend was observed for different W devices as well [see S1 in the Supporting Information], indicating that P_{BD} scaled linearly with the footprint area ($L \times W$). Based on this, we initially assumed that the BP channel was subjected to Joule heating and that heat energy was spread out along the in-plane and out-of-plane directions toward the BP electrode (Cr/Au) and BP–dielectric (SiO_2) interfaces, respectively. Additionally, it seems that the former interface may serve as a more efficient heat sink than the latter interface due to better thermal coupling of metallic contacts with the BP flake compared to SiO_2. As a result, the edges of the channel cooled off, and the dissipated heat is trapped along the BP–SiO_2 interface, inducing thermal stresses inside the channel at a high electric field. This explains the linear trend between P_{BD} and the channel cross-section. Further details about this understanding are provided below.

Owing to the 2D geometry of BP, its in-plane κ value is larger than that of the out-of-plane value, mainly due to strong in-plane covalent bonds and weak van der Waals interactions along the c-axis, respectively, resulting in effective lateral thermal power propagation.[11] This seems to contradict our above speculation, where we assumed dominant heat spreading and trapping would occur in the out-of-plane direction. This contradiction suggests that κ is not the only parameter that influences the heat dissipation direction, but device dimensions,[19] the nature of the interface,[21] and surface conditions[2–4] may also affect the thermal spreading caused by Joule heating. From a geometry perspective, the out-of-plane cross-sectional area ($L \times W$) of BP devices is normally several orders larger than the in-plane cross-sectional area ($t \times W$), which results in a

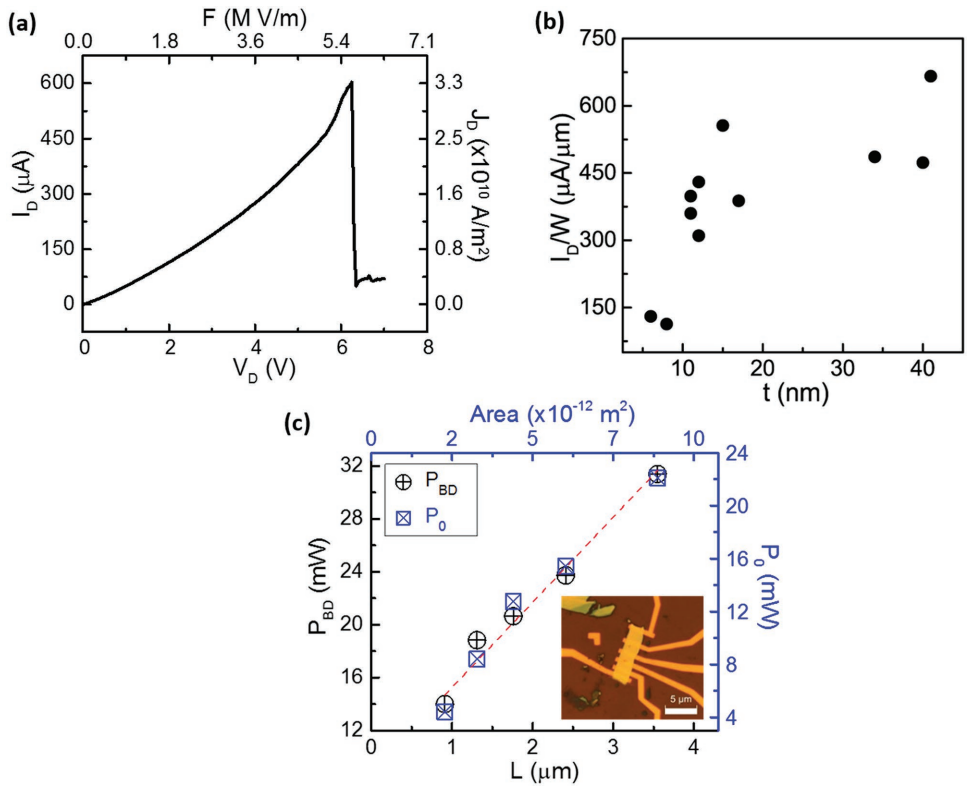

Figure 2. Electrical breakdown of BP and its dependency on device dimensions. a) The current density of the back gate BP FET device at zero gate bias plotted against applied bias and electrical field. b) Thickness-dependent maximum current level of various ≈1 μm long BP-FETs. c) Breakdown power (P_{BD} and $P_0 = P_{BD} - I_{BD}^2 R_c$) obtained from different channel length devices fabricated on the same BP flake. The top axis denotes the corresponding cross-sectional area ($L \times W$). The inset shows an OM image of the device.

higher thermal conductance along the out-of-plane direction. Furthermore, at elevated lattice temperature, the higher frequency optical branches were excited, leading to an enhanced contribution of optical phonon branches and softening of flexural phonon branches (*z*-direction acoustic modes). This resulted in a suppressed κ of BP, which in turn impeded the lateral heat propagation.[12] This observation suggests that the hot carriers were spatially confined near the center of the BP channel at high lattice temperature, inducing a temperature plateau (hotspots) inside the channel.[23] In short, due to centrally localized thermal carriers and the ultrathin BP flake, the net thermal power dissipation occurs primarily toward the Si substrate. As mentioned previously, thicker BP flakes exhibited higher κ values and less surface scattering when compared to thinner flakes.[9] Therefore, multilayer BP flakes with shorter and/or narrower channels would be desirable for effective heat spreading in operational electronic devices.

As mentioned earlier, the formation of thermally abrupt junctions masks the thermal transport in nanomaterials. Likewise, interfacial thermal properties greatly influence the operation of miniaturized devices and must be fully understood. Previous studies on 2D materials like graphene and MoS_2 supported on SiO_2 suggest that the oxide–channel interface is a bottleneck to the heat dissipation mainly due to weak thermal and structural coupling.[19,24] Special experimental setups were prepared in previous works to extract the interfacial thermal conductance (G).[10,25–27] However, in this study, we employed a highly robust analytical model based on electrical and thermal transport to extract G per unit area of BP–dielectric interfaces[3,16,28]

$$\begin{aligned} Q'' &= G\Delta T \\ P_0 &= G(T_{BD} - T_0) \times A \end{aligned} \tag{1}$$

where T_{BD} is the breakdown temperature of the BP FET and T_0 is room temperature. Q'' is the heat transfer per unit area, and P_0 is the breakdown power of the BP device excluding power dissipated along the contacts, i.e., $P_0 = P_{BD} - I^2_{BD} R_c$. Here, R_c is the contact resistance of the BP device extracted using the transfer length method [see S2 in the Supporting Information]. We obtained a G of ≈7.3 MW m^{-2} K^{-1} for the BP–SiO_2 interface by linearly fitting the data in Figure 2c and using $T_{BD} \approx 520$ K for the BP FET on SiO_2. We prepared more than six different thickness BP devices and extracted their corresponding G values, which spanned the range of 2–10 M W m^{-2} K^{-1}. This variation is probably due to different BP–SiO_2 interface conditions, surface qualities, and BP flake thicknesses. Similarly, we deduced G for different BP–dielectric interfaces, as shown in S3 in the Supporting Information. It seems that the value of G mainly depends on the nature of the particular interface rather than the thermal properties of dielectric material. A similar understanding was previously realized for other nanomaterials and dielectric interfaces.[2,3,16] However, the extracted values were very close to the reported values for other 2D materials like MoS_2 and $MoSe_2$ on SiO_2, and they were around one order

smaller than the reported values for graphene–SiO_2 interfaces.[10,25–27] Thermal decay length (λ_{Th}) of metal electrode is another parameter that indicates the dominant path of thermal power dissipation in a device. For example, if the channel is much longer than λ_{Th}, heat will be mainly dissipated through the underlying substrate, while for comparatively equal or shorter channels it will predominantly sink through metallic electrodes.[24,28] λ_{Th} is analogous to the electrical transfer length and can be extracted as

$$\lambda_{Th} = \sqrt{\kappa t / G} \tag{2}$$

Here, κ and t are the in-plane thermal conductivity and thickness of the BP channel, respectively. Using κ_{avg} = 28.8 W m^{-1} K^{-1}[9] and t = 41 nm for our representative device, we extracted a value of $\lambda_{Th} \approx$ 400 nm. Our smallest channel is more than two times longer than λ_{Th}, and this further confirms that most of the power was vertically dissipated along the BP–SiO_2 interface. The readers should note that the above analytical model can only be used for devices with small R_c, but it may not hold well for semiconducting TMDCs that have a relatively large R_c.[29]

Owing to their high surface-to-volume ratio, 2D materials are highly sensitive to their immediate environment. Therefore, their electronic and photonic behavior can be easily altered by dielectric engineering. As explained above, the thermal energy is primarily transferred to the Si substrate through the dielectric during device operation. Likewise, devices fabricated on SiO_2 are subjected to thermal spreading problems due to its poor thermal conductivity ($\kappa \approx$ 1.4 W m^{-1} K^{-1}) and corrugated surface.[21] Therefore, integration of thermally and structurally favorable dielectric materials instead of SiO_2 may greatly suppress these adverse effects and help keep the device cool during high field operation.

hBN is a wide-band-gap (5.8 eV) layered dielectric material having a pristine flat surface, a good dielectric constant (≈3.5), a high in-plane κ (≈360 W m^{-1} K^{-1}), and large surface optical phonon modes; these properties indicate that hBN is a strong candidate for use in 2D devices.[17,30] Previously, hBN was integrated with graphene and TMDCs for enhancing charge carrier transport.[30,31] Recently, hBN was integrated with BP as a capping layer[32] and an electrical performance booster for low field operations.[33,34] Therefore, we employed it as an alternative dielectric material for high-field transport in BP devices. To this end, we exfoliated few-layer hBN flakes onto SiO_2 and mechanically stacked ≈150 nm thick BP flakes over it using a dry transfer technique.[30,35] The BP flake was partially stacked over the hBN, as shown in **Figure 3**a, and two different devices with the same device dimensions were fabricated along the same in-plane direction of BP flake (i.e., the zigzag direction), as confirmed by polarized Raman spectroscopy[36] to ensure a fair comparison. First, we characterized both devices at lower

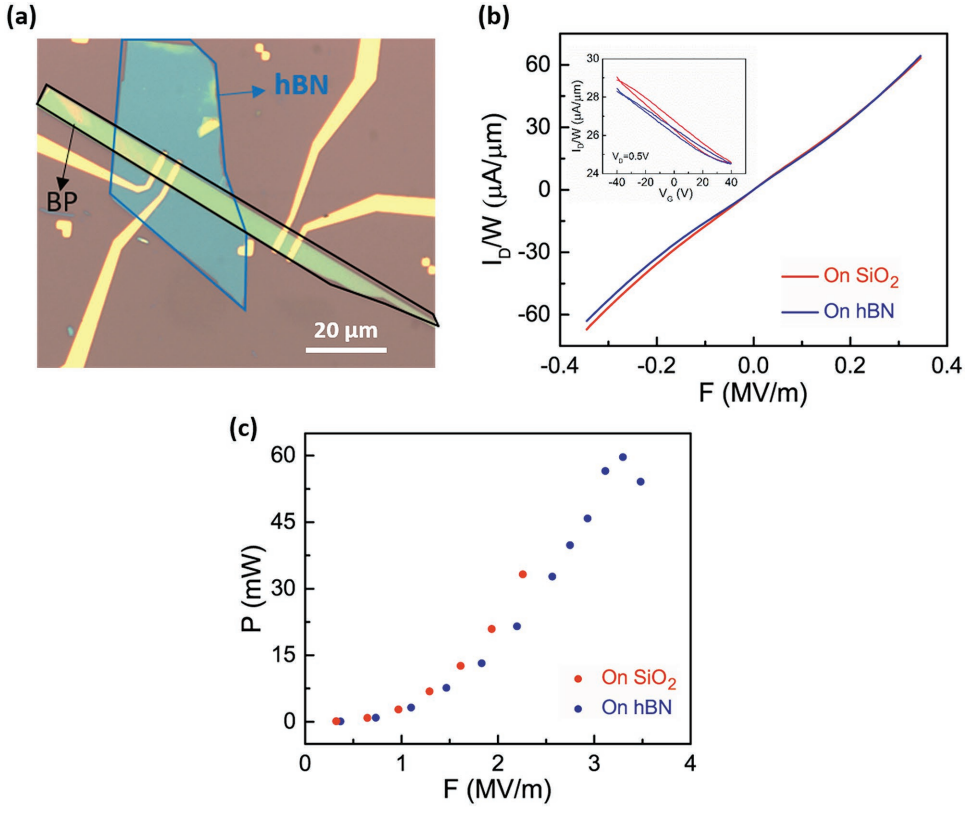

Figure 3. Dielectric engineering to multilayer BP device. a) Optical microscope image of BP flake partly stacked over hBN. The black and blue bordered areas indicate ≈150 nm thick BP and multilayer hBN regions, respectively. b) Low field electrical transport behavior of BP device on SiO_2 and hBN at V_G = 0. The inset shows their corresponding hysteresis plots at V_D = 0.5 V. c) The obtained electrical power plotted against an applied electrical field for a BP device on SiO_2 and hBN.

electrical fields, as shown in Figure 3b. We did not observe any significant change in low-field electrical characteristics for SiO_2- and hBN-supported BP devices. We attributed the observed stubborn behavior of BP to the fact that the optical phonon scattering of BP in a low field may be the dominant scattering mechanism. This behavior may also be due to the weak charge screening effect caused by thicker BP flakes in our particular case. Previously, researchers reported that BP devices on hBN substrates showed a slight improvement in current level after a double annealing processing.[34] Based on this report, we believe that improvement can be partially attributed to annealing effects rather than the hBN dielectric alone. Afterwards, we slowly increased the applied electric field and, to our surprise, we observed an obvious change in higher electrical field transport for given devices. Our BP device on hBN exhibited a higher maximum power density and electric field sustainability than that on SiO_2, as shown in Figure 3c. The BP device on SiO_2 exhibited an ultimate power of 33.25 mW at a maximum electric field of 2.25 MV m^{-1}, while a nearly twofold increase in power value (59.63 mW) and a comparatively larger field of 3.47 MV m^{-1} were realized on the hBN dielectric.

We repeated the experiment on more than four different devices and observed a two- to threefold increase in maximum power values. These superior high-field transport values were attributed to efficient thermal dissipation of BP devices on hBN compared to that on SiO_2. Structurally, hBN had an atomically flat and inert surface, while that of SiO_2 is highly corrugated and rough. Acoustic phonons, the dominant heat carriers in semiconducting materials, are more sensitive to interface scattering than their optical companions.[2] As such, the rough surface of SiO_2 may greatly limit the thermal transport in the device, whereas relatively smooth heat conduction can be obtained using hBN. Additionally, hBN has a ≈250-fold higher κ and twofold higher surface optical phonon energy compared to SiO_2, which enabled relatively better thermal coupling of hBN to BP. This further facilitated thermal spreading during high field operation.

To quantitatively analyze the impact of dielectric engineering on the high field transport of the BP device, we performed micro-Raman spectroscopy to extract the local temperature increase in the device. Micro-Raman spectroscopy is a non-invasive approach for determining the phonon temperature, and it has previously been employed in 2D materials like graphene[23,37] and BP.[14] Further details about our micro-Raman setup can be found elsewhere.[23] The crystalline multilayer BP exhibited three dominant Raman peaks. The two in-plane modes of A^2g and B_2g represent atomic oscillations along the zigzag and armchair directions, respectively, and one out-of-plane mode, A^1g, depicts the z-direction lattice vibration.[14,36,38] We performed Stokes (positive) and anti-Stokes (negative) Raman spectroscopy on our BP devices on SiO_2 and hBN dielectrics under an applied voltage as shown in **Figure 4**a,b respectively. The measured zero bias (V_D = 0 V) Raman peaks at ± 365, ± 442, ± 470 cm^{-1} were attributed to the corresponding A^1g, B_2g, and A^2g phonon modes of crystalline BP. Further, we gradually increased the applied bias and recorded the Raman

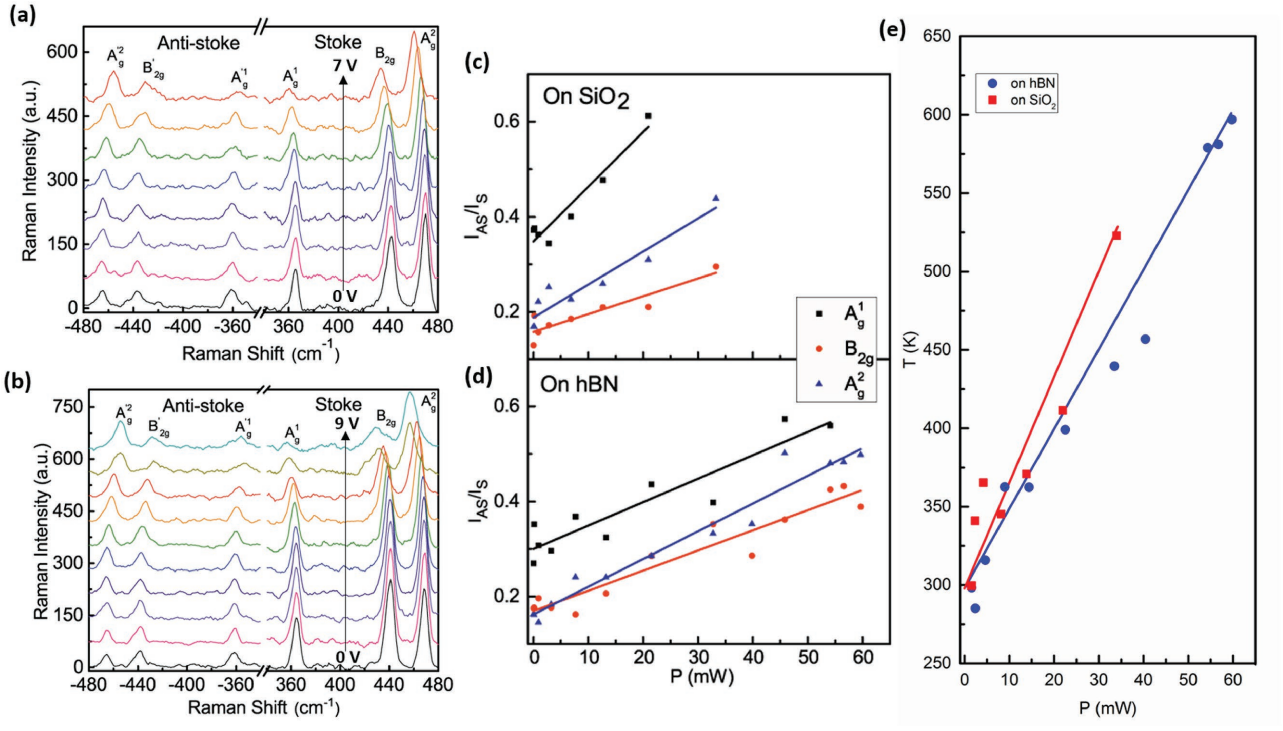

Figure 4. Temperature extraction from micro-Raman spectroscopy. a,b) The obtained Stokes and anti-Stokes Raman spectra of BP device on SiO_2 and hBN, respectively, at different applied bias conditions. c,d) represent the ratio of deconvolution Stokes and anti-Stokes Raman peaks from (a,b), respectively, plotted as a function of applied power. e) The calculated phonon temperature of BP device on SiO_2 and hBN at a given power density. The lines represent analytically computed temperatures and the solid points are the experimentally determined temperatures from micro-Raman signals. Note that this temperature is extracted by comparing the A^2g phonon modes.

signal so as to observe Raman peak softening with increasing V_D for BP devices on both the dielectric materials. It should be noted that no gate bias was applied during Raman measurements since the thicker BP flakes usually showed immunity toward gating, mainly due to weak charge screening. Thus, the spectral shift in Raman spectra is solely caused by electrical heating of BP lattice. Generally, the intrinsic softening of Raman peaks due to increase in flake temperature is attributed to the thermal expansion of lattice and an-harmonic phonon coupling.[36] Therefore, a clear red shift in Raman spectra of BP lattice, as shown in Figure 4a,b, is mainly realized due to self-heating of BP flake by applied electrical bias. It is important to note that the similar shift in Raman modes was realized by direct thermal heating of BP flake as well.[36] The further details about spectral peaks position shift and related extraction of electrical heating coefficients of specific Raman modes of multilayer BP are given in S4 in the Supporting Information. The deconvoluted intensity ratios of Stokes (I_S) and anti-Stokes (I_{AS}) peaks were plotted as a function of applied electrical power as shown in Figure 4c,d on SiO_2 and hBN substrates, respectively. As shown, we observed a linearly increasing trend for all the three Raman modes. This ratio can be translated to a temperature by using Equation (3)[23]

$$\frac{I_{AS}}{I_S}\alpha C\exp\left(-\frac{E_{op}}{k_B T_{ph}}\right) \tag{3}$$

Here, T_{ph} is the phonon temperature and E_{op} is the optical phonon energy of each Raman peak: A^1g = 45.19 meV, B_2g = 54.68 meV, and A^2g = 58.15 meV. C is the measured pre-factor due to the CCD response and optics, which were carefully calibrated. We obtained an operating temperature at a given applied power value for the A^2g mode by using the ratios of Stokes and anti-Stokes intensities from Figure 4c,d in Equation (3), as shown in Figure 4e. In addition to this, we employed an analytical model based on heat diffusion equation to compute the operating temperature (see S5, S6 in the Supporting Information). The obtained results are shown in Figure 4e by solid lines, and they fit well with our experimentally determined temperature numbers. However, from analytical and experimental temperature results we observed that BP on hBN showed relatively lower operating temperatures (i.e., cooler device operation) than that of SiO_2 under the same applied field conditions. This indicates efficient heat dissipation in the hBN supported BP device.

Similarly, we obtained peak operating temperatures of 520 and 600 K at the breakdown point for the BP device on SiO_2 and hBN substrates, respectively. SiO_2 is known for enhancing surface scattering, mainly due to surface polar optical phonon scattering via remote-phonon interactions and charged impurity scattering, which cause hot carrier relaxation and eventually affect the local temperature in the device.[23] In contrast, the atomic level flatness of hBN enables intimate thermal contact with BP, causing better phonon–phonon interactions between them, which ensure relatively cooler device operation. This observation further confirmed that BP on hBN can withstand a higher maximum power density and operating temperature due to efficient cooling of a device at high field operation. Our observed breakdown temperature values on both substrates were smaller than previously extracted for BP, i.e., 757 K in Ref. [14]. We think this difference may be due to different quality and thicknesses of BP used, different processing and operating conditions adopted, and more notably different dielectrics than were previously used (200 nm indium tin oxide and 100 nm Al_2O_3). Nonetheless, at such high temperature, the crystalline black phosphorus flake may have already changed to amorphous red phosphorus.[39]

Finally, we inspected the devices after electrical breakdown under an optical microscope. Interestingly, we observed that the BP device on SiO_2 experienced cracks in the vicinity of the electrode, while it is located along the center of the channel for hBN as shown in **Figure 5**a. We further confirmed this anomaly in BP devices on SiO_2 by using AFM, as shown in Figure 5b. The observed crack position from the AFM image indicates that a hotspot was induced ≈450 nm away from the metal electrode, which is also consistent with the thermal decay length of metal electrode ($\lambda_{Th} \approx 400$ nm). Based on the location of thermally induced cracks, we speculated that thermal spreading was nonuniform for BP devices on SiO_2, whereas it seemed more homogeneous on an hBN substrate.

The position of hotspots on BP devices on SiO_2 is also of interest. It was previously reported that the thermally induced trapped charges in SiO_2 resulted in an abrupt doping profile below the 2D material.[40–42] Therefore, a hotspot was induced near regions of low carrier density (biased contact). This may be the reason that we observed thermally induced cracking near the metallic electrode (drain) on SiO_2. Based on the above discussion, it is clear that the poor structural and thermal properties of SiO_2 not only impeded thermal distribution that masked device operating temperature, but also resulted in uneven heat spreading that caused rupture near the metallic electrode. On the other hand, better structural and thermal coupling of hBN with BP helped realize homogenous thermal spreading while enabling cooler device operation. This allowed us to achieve centrally localized hotspots and relatively higher sustainability of breakdown power density compared to devices on SiO_2. In the future, this inhomogeneity can be further studied in further detail by employing spatial resolution techniques, e.g., scanning thermal microscopy, infrared spectroscopy,[43] and scanning Joule microscopy.[44] Our analysis demonstrated that hBN not only effectively protected BP from environmental perturbations and improved performance under low fields, but it is also a favorable dielectric material for high field operations.

3. Conclusion

In conclusion, we applied breakdown thermometry to study the power dissipation in BP FETs. We found that multilayer BP exhibited a higher current density than that of multilayer MoS_2 in a back gate device structure. Moreover, the interfacial thermal conductance between BP–dielectric interface was extracted by implementing a simple analytical approach. Finally, the dielectric material greatly influenced high-field operation. Similarly, efficient device cooling was achieved by employing hBN as a dielectric for BP devices instead of SiO_2.

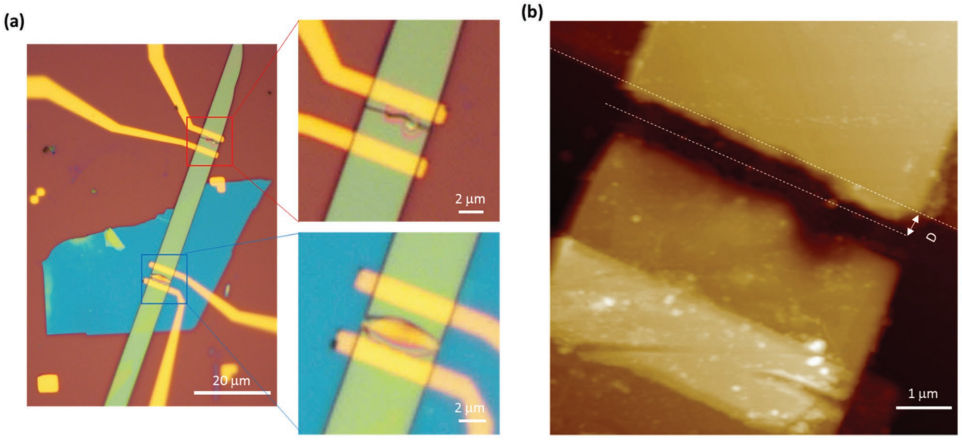

Figure 5. Optical and atomic force microscopy of BP devices after electrical breakdown. a) Optical microscope image of BP devices on SiO_2 and hBN substrate after electrical breakdown. The red- and blue-colored squares indicate the SiO_2 and hBN supported BP devices respectively b) AFM image of ≈150 nm thick broken BP device on SiO_2 substrate, where *D* denotes the distance between the electrode and hotspot.

4. Experimental Section

Device Fabrication: Multi-layer BP flakes were placed on a p-doped Si substrate capped with thermally grown 285 nm SiO_2 in an Ar atmospheric glove box having oxygen and moisture levels <1 ppm. Candidate flakes were targeted by optical contrast, and an electron beam resist polymer polymethyl methacrylate (PMMA) was coated on the substrates inside an environmentally controlled glove box. Electrodes were patterned via electron beam lithography and 5/50 nm-thick Cr/Au metal layers were deposited by electron beam deposition followed by lift-off in acetone to remove excessively deposited metal. A schematic of the simple two-terminal back gate BP FET device is shown in Figure 1a, and an optical microscopy (OM) image of an ≈11 nm-thick BP device is shown in Figure 1b. The thickness of the BP flakes was measured using atomic force microscopy (AFM). An error of ±1 nm is appropriate for these measurements due to the collection of moisture over the BP surface. During the fabrication process, extra efforts were made to minimize BP exposure to the ambient environment to ensure high quality BP devices. Soon after lift-off, electrical measurements were carried out in a vacuum environment, and the measurements led to subsequent breakdown of BP devices. Therefore, the total environmental exposure was very short; hence, the probability of oxidation of the BP devices was very low. The authors recently studied the stability and effective passivation of BP flakes elsewhere.[45]

Micro-Raman Spectroscopy: Micro-Raman spectroscopy was acquired using the 514.5 nm Ar laser with a power of 300 μW and spot size of 1 μm under vacuum (≈10^{-5} Torr) with applied electric field to multilayer BP devices. The authors used a long working distance ×50 object lens (Olympus LMPLFN50×) and spectrometer (Princeton Instrument, eXcelon-100B, 1800 groove mm^{-1} grating) with 30 s exposure time.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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[1] G. R. Bhimanapati, Z. Lin, V. Meunier, Y. Jung, J. Cha, S. Das, D. Xiao, Y. Son, M. S. Strano, V. R. Cooper, L. Liang, S. G. Louie, E. Ringe, W. Zhou, S. S. Kim, R. R. Naik, B. G. Sumpter, H. Terrones, F. Xia, Y. Wang, J. Zhu, D. Akinwande, N. Alem, J. A. Schuller, R. E. Schaak, M. Terrones, J. A. Robinson, *ACS Nano* **2015**, *9*, 11509.
[2] A. A. Balandin, *Nat. Mater.* **2011**, *10*, 569.
[3] E. Pop, *Nano Res.* **2010**, *3*, 147.
[4] A. L. Moore, L. Shi, *Mater. Today* **2014**, *17*, 163.
[5] L. Li, Y. Yu, G. J. Ye, Q. Ge, X. Ou, H. Wu, D. Feng, X. H. Chen, Y. Zhang, *Nat. Nanotechnol.* **2014**, *9*, 372.
[6] H. Liu, A. T. Neal, Z. Zhu, Z. Luo, X. Xu, D. Tománek, P. D. Ye, *ACS Nano* **2014**, *8*, 4033.
[7] F. Xia, H. Wang, Y. Jia, *Nat. Commun.* **2014**, *5*, 5458.
[8] Y. Cai, G. Zhang, Y.-W. Zhang, *Sci. Rep.* **2014**, *4*, 6677.
[9] Z. Luo, J. Maassen, Y. Deng, Y. Du, R. P. Garrelts, M. S. Lundstrom, P. D. Ye, X. Xu, *Nat. Commun.* **2015**, *6*, 9572.
[10] X. Zhang, D. Sun, Y. Li, G.-H. Lee, X. Cui, D. Chenet, Y. You, T. F. Heinz, J. Hone, *ACS Appl. Mater. Interfaces* **2015**, *7*, 25923.
[11] H. Jang, J. D. Wood, C. R. Ryder, M. C. Hersam, D. G. Cahill, *Adv. Mater.* **2015**, *27*, 8017.
[12] G. Qin, Q.-B. Yan, Z. Qin, S.-Y. Yue, M. Hu, G. Su, *Phys. Chem. Chem. Phys.* **2015**, *17*, 4854.
[13] S. J. Choi, B.-K. Kim, T.-H. Lee, Y. H. Kim, Z. Li, E. Pop, J.-J. Kim, J. H. Song, M.-H. Bae, *Nano Lett.* **2016**, *16*, 3969.
[14] M. Engel, M. Steiner, S.-J. Han, P. Avouris, *Nano Lett.* **2015**, *15*, 6785.
[15] T. Low, M. Engel, M. Steiner, P. Avouris, *Phys. Rev. B* **2014**, *90*, 081408.
[16] E. Pop, D. A. Mann, K. E. Goodson, H. Dai, *J. Appl. Phys.* **2007**, *101*, 093710.
[17] I. Jo, M. T. Pettes, J. Kim, K. Watanabe, T. Taniguchi, Z. Yao, L. Shi, *Nano Lett.* **2013**, *13*, 550.
[18] O. Lopez-Sanchez, D. Lembke, M. Kayci, A. Radenovic, A. Kis, *Nat. Nanotechnol.* **2013**, *8*, 497.
[19] R. Yang, Z. Wang, P. X. L. Feng, *Nanoscale* **2014**, *6*, 12383.

[20] D. Lembke, A. Kis, *ACS Nano* **2012**, *6*, 10070.
[21] J. Yu, G. Liu, A. V. Sumant, V. Goyal, A. A. Balandin, *Nano Lett.* **2012**, *12*, 1603.
[22] D. Qu, X. Liu, F. Ahmed, D. Lee, W. J. Yoo, *Nanoscale* **2015**, *7*, 19273.
[23] Y. D. Kim, H. Kim, Y. Cho, J. H. Ryoo, C.-H Park, P. Kim, Y. S. Kim, S. Lee, Y. Li, S.-N. Park, Y. S. Yoo, D. Yoon, V. E. Dorgan, E. Pop, T. F. Heinz, J. Hone, S.-H. Chun, H. Cheong, S. W. Lee, M.-H. Bae, Y. D. Park, *Nat. Nanotechnol.* **2015**, *10*, 676.
[24] Y. K. Koh, M.-H. Bae, D. G. Cahill, E. Pop, *Nano Lett.* **2010**, *10*, 4363.
[25] Z. Chen, W. Jang, W. Bao, C. N. Lau, C. Dames, *Appl. Phys. Lett.* **2009**, *95*, 161910.
[26] K. F. Mak, C. H. Lui, T. F. Heinz, *Appl. Phys. Lett.* **2010**, *97*, 221904.
[27] A. Taube, J. Judek, A. Łapińska, M. Zdrojek, *ACS Appl. Mater. Interfaces* **2015**, *7*, 5061.
[28] Y. D. Kim, M.-H. Bae, *InTech*, **2016**, DOI:10.5772/64051.
[29] F. Ahmed, M. S. Choi, X. Liu, Y. J. Yoo, *Nanoscale* **2015**, *7*, 9222.
[30] C. R. Dean, A. F. Young, I. Meric, C. Lee, L. Wang, S. Sorgenfrei, K. Watanabe, T. Taniguchi, P. Kim, K. L. Shepard, J. Hone, *Nat. Nanotechnol.* **2010**, *5*, 722.
[31] M. S. Choi, D. Qu, D. Lee, X. Liu, K. Watanabe, T. Taniguchi, W. J. Yoo, *ACS Nano* **2014**, *8*, 9332.
[32] R. A. Doganov, E. C. T. O'Farrell, S. P. Koenig, Y. Yeo, A. Ziletti, A. Carvalho, D. K. Campbell, D. F. Coker, K. Watanabe, T. Taniguchi, A. H. C. Neto, B. Ozyilmaz, *Nat. Commun.* **2015**, *6*, 7647.
[33] L. Li, G. J. Ye, V. Tran, R. Fei, G. Chen, H. Wang, J. Wang, K. Watanabe, T. Taniguchi, L. Yang, X. H. Chen, Y. Zhang, *Nat. Nanotechnol.* **2015**, *10*, 608.
[34] R. A. Doganov, S. P. Koenig, Y. Yeo, K. Watanabe, T. Taniguchi, B. Ozyilmaz, *Appl. Phys. Lett.* **2015**, *106*, 083505.
[35] H.-M. Li, D. Lee, D. Qu, X. Liu, J. Ryu, A. Seabaugh, W. J. Yoo, *Nat. Commun.* **2015**, *6*, 6564.
[36] S. Zhang, J. Yang, R. Xu, F. Wang, W. Li, M. Ghufran, Y.-W. Zhang, Z. Yu, G. Zhang, Q. Qin, Y. Lu, *ACS Nano* **2014**, *8*, 9590.
[37] M. Freitag, M. Steiner, Y. Martin, V. Perebeinos, Z. Chen, J. C. Tsang, P. Avouris, *Nano Lett.* **2009**, *9*, 1883.
[38] Z. Guo, H. Zhang, S. Lu, Z. Wang, S. Tang, J. Shao, Z. Sun, H. Xie, H. Wang, X.-F. Yu, P.K. Chu, *Adv. Funct. Mater.* **2015**, *25*, 6996.
[39] X. Liu, J. D. Wood, K.-S. Chen, E. Cho, M. C. Hersam, *J. Phys. Chem. Lett.* **2015**, *6*, 773.
[40] H.-Y Chiu, V. Perebeinos, Y.-M. Lin, P. Avouris, *Nano Lett.* **2010**, *10*, 4634.
[41] Y. D. Kim, M.-H. Bae, J.-T. Seo, Y. S. Kim, H. Kim, J. H. Lee, J. R. Ahn, S. W. Lee, S.-H. Chun, Y. D. Park, *ACS Nano* **2013**, *7*, 5850.
[42] G. Rao, M. Freitag, H.-Y. Chiu, R. S. Sundaram, P. Avouris, *ACS Nano* **2011**, *5*, 5848.
[43] M.-H. Bae, Z.-Y. Ong, D. Estrada, E. Pop, *Nano Lett.* **2010**, *10*, 4787.
[44] K. L. Grosse, M.-H. Bae, F. Lian, E. Pop, W. P. King, *Nat. Nanotechnol.* **2011**, *6*, 287.
[45] D. Yue, D. Lee, Y. D. Jang, M. S. Choi, H. J. Nam, D.-Y. Jung, W. J. Yoo, *Nanoscale* **2016**, *8*, 12773.